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15
Citations (Scopus):
727

Supervised MSc Theses

#	Thesis title	By	Date
1	Design Space Exploration of Hardware Accelerator for Recurrent Deep Learning on FPGA Devices	Ali Mohammad Pour & Morteza Saheb Zamani	April 2021
2	proposing a reconfigurabchitecture to detect web application attacks	Ali Suzangar & Morteza Saheb Zamani	January 2021
3	A Technique for Partitioning of Circuit in Scalable Quantum Computers	Bahare Jalili & Morteza Saheb Zamani	August 2020
4	Designing an Embedded System for Activity Recognition Using a Surveillance Camera	Sahar Darafsh & Morteza Saheb Zamani	June 2020
5	Hardware Trojan Horse Detection on Commercial Off-The-Shelf Chips	Jamileh Behzadi & Morteza Saheb Zamani	February 2019
6	Proposing a Placement Method to facilitate Hardware Trojan Detection	Milad Sharbati & Morteza Saheb Zamani	June 2018
7	Improving Trustability of RTL IP Cores	Ramin Norouzzadeh & Morteza Saheb Zamani	June 2018
8	Real-time task scheduler on FPGA	Pouya Mahmoody & Morteza Saheb Zamani	February 2018
9	Finding relevant subset of elementary flux modes in metabolic networks	Faridoddin Shafi & Morteza Saheb Zamani	February 2018
10	Hierarchical Decomposition of Metabolic Networks for Calculation of Elementary Flux Modes	Sina Ghadermarzi & Morteza Saheb Zamani	February 2017

11	Detection of functional Hardware Trojan Horse in reconfigurable chips Bitstream	Seyedmohammadmehdi Sharifonasabi & Morteza Saheb Zamani	February 2017
12	fpga-based reconfigurable cpgs for bipedal walking robot	Elham Ebrahimi & Morteza Saheb Zamani	July 2016
13	A Hardware Architecture for Computing Elementary Flux Modes in Metabolic Networks	Seyede Marzieh Hashemipour Nazari & Morteza Saheb Zamani	February 2016
14	Soft IP Protection In FPGA	Mehrnoush Moradi Haghighi & Morteza Saheb Zamani	October 2015
15	Optimizing quantum cost of reversible circuits using garbage bits	Mehrdad Goharibelili & Morteza Saheb Zamani	September 2015
16	Optimization of Quantum Circuits Using One Way Quantum Computing	Maryam Eslamy & Morteza Saheb Zamani	October 2014
17	Hardware Trojan horses detection using multi VDD design	Farzaneh Bordbar & Morteza Saheb Zamani	October 2014
18	a Region-Aware Testing Method for Hardware Trojan Detection	Mohammad Mahdi Fathollahi Nanekaran & Morteza Saheb Zamani	March 2014
19	search based design of a library for one-way quantum computing model	Ehsan Varvaie & Morteza Saheb Zamani	February 2014
20	Hardware Trojan horse Detection by Varying Supply Voltage Levels	Behnam Omidi & Morteza Saheb Zamani	October 2013
21	analyzing the resistance of design for hardware trust techniques against attackers neutralizing efforts	Shirin Alsadet Aalami & Morteza Saheb Zamani	June 2013
22	improving the performance of network on chips by changing the structure of VIPs	Masoud Ganjkhany & Morteza Saheb Zamani	June 2013
23	accelerating network motif finding algorithm using GPU implementation	Ahmadreza Jahani & Morteza Saheb Zamani	February 2013
24	an efficient simulation of one-way Quantum computing	Eesa Nikahd & Morteza Saheb Zamani	October 2012
25	A test approach for detecting malicious hardware	Arash Nejat & Morteza Saheb Zamani	October 2012
26	acceleration of protein tertiary structure comparion algorithm using FPGA	Somayeh Kashi & Morteza Saheb Zamani	July 2012
27	ensuring hardware trust via trustworthy and trojan free intllectual property cores	Salar Sayedebrahimi & Morteza Saheb Zamani	May 2012
28	vpr tool algoritm optimising	Habib Ollah Seifi & Morteza Saheb Zamani	April 2012
29	a system-level architecture for heterogeneous 3D-FPGAs	Sahar Mousavi Khoee & Morteza Saheb Zamani	February 2012
30	proposing a combined physical unclonable function	Mohnoosh Borjian Boroujeni & Morteza Saheb Zamani	February 2012
31	multi-objective synthesis of reversible logic circuits	Mona Arabzadeh & Morteza Saheb Zamani	October 2011

32	FPGA architecture improvment for timing yield enhancemant in presence of process variation	Fatemehsadat Pourhashemi Naeeni & Morteza Saheb Zamani	February 2011
33	temperature-aware routing in 3-D FPGAs	Amin Ezhdehakosh & Morteza Saheb Zamani	February 2011
34	a scheduling algorithm for quantum circuits to reduce execution time	Hamidreza Lotfalizadeh & Morteza Saheb Zamani	February 2011
35	3D FPGA Switch box Design for Area Reduction	Seyyed Ahmad Razavi Majomard & Morteza Saheb Zamani	July 2010
36	Proposing a New Method for Scheduling Quantum Circuits in ion-trap technology with the aim of reducing the operation Time of the Circuit	Maryam Yazdani & Morteza Saheb Zamani	July 2010
37	Process Variation –aware Placement Algorithm for leakage Power Reduction in FPGAs	Behzad Salami & Morteza Saheb Zamani	July 2010
38	place and route in three dimensional fpgas	Seyyed Hassan Moallem Pour & Morteza Saheb Zamani	May 2010
39	Design of a Fault-Tolerant Routing Connection Architecture for SRAM-Based FPGAs	Hassan Ebrahimi & Morteza Saheb Zamani	December 2009
40	delay variability modeling in FPGA circuits for physical design	Mahdi Nabiyouni & Morteza Saheb Zamani	July 2009
41	statically multiple output custom instruction generation for configurable processors	Mohammad Hassan Kefayati & Morteza Saheb Zamani	July 2009
42	a method to reduce congestion during partitioning- based placement	Hosein Shafiei & Morteza Saheb Zamani	May 2009
43	A hardware core for detecting and generating custom instructions and reconfiguring architecture dynamically	Hasan Asgharian & Morteza Saheb Zamani	April 2009
44	Emulation of Quantum circuits with FPGA	Mahdi Aminian & Morteza Saheb Zamani	December 2008
45	A NEW METHODOLOGY TO ESTIMATE AND REDUCE CROSSTALK IN PLACEMENT BASED ON A MULTILEVEL ROUTER	Arash Mahdizadeh & Morteza Saheb Zamani	March 2008
46	A STATISTICAL APPROACH FOR DELAY AND POWER OPTIMIZATION USING AN EVOLUTIONARY ALGORITHM	Minoo Mirsaeedi & Morteza Saheb Zamani	February 2008
47	RETIMING DRIVEN PLACEMENT FOR PERFORMANCE OPTIMIZATION	Adel Dokhanchi & Morteza Saheb Zamani	February 2008
48	A NEW APPROACH TO PARTITIONING FOR REGISTER PLACEMENT TO OPTIMIZE CLOCK NETWORK	Zahra Lak Chalsepari & Morteza Saheb Zamani	August 2007
49	AN INTEGRATED APPROACH TO THE PLACEMENT AND ROUTING TO REDUCE TOTAL WIRE LENGTH AND CONGESTION	Mostafa Rezvani & Morteza Saheb Zamani	June 2007
50	TECHNOLOGY REMAPPING WITH ROUTING CONGESTON REDUCTION CONSIDERATION	Abbas Ali Arabi Mazraeh Shahi & Morteza Saheb Zamani	June 2007
51	NON-TREE CLOCK ROUTING FOR REDUCING DELAY UNCETAINTY	Maryam Taajobian & Morteza Saheb Zamani	April 2007
52	A NEW METHOD FOR BUFFER INSERTION TO REDUCE INTERCONNECT DELAYS IN VLSI CIRCUITS	Hamidreza Kheirabadi & Morteza Saheb Zamani	December 2006

Books

#	Title	Author(s)	Publisher country	publication date	version
	Portal Records				
1	Computer-Aided Digital Systems Design	Morteza Saheb Zamani	Iran (Islamic Republic of)	June 2019	1

Journal Papers

Portal Records

1. Eesa Nikahd, Naser Mohammadzadeh, Mehdi Sedighi, Morteza Saheb Zamani, "Automated window-based partitioning of quantum circuits", PHYSICA SCRIPTA, March 2021 Vol. 96, Num. 3, Page 1-19, March 2021,

2. Mona Arabzadeh, Mehdi Sedighi, Morteza Saheb Zamani, Sayed-Amir Marashi, "A system architecture for parallel analysis of flux-balanced metabolic pathways", COMPUTATIONAL BIOLOGY AND CHEMISTRY, June 2020 Vol. 88, Num. 107309, Page 1-15, June 2020,

3. Ghobad Zarrinchian, Morteza Saheb Zamani, "Combinational Counters: A Low Overhead Approach to Address DPA Attacks", JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, May 2020 Vol. 29, Num. 6, Page 1-19, May 2020,

4. Mohammad Hadi Mottaghi Khezri, Mehdi Sedighi, Morteza Saheb Zamani, "Aging Mitigation in FPGAs Considering Delay, Power and Temperature", IEEE TRANSACTIONS ON RELIABILITY, June 2019 Vol. 68, Num. 2, Page 0-0, June 2019,

5. Maryam Eslamy, Mahboobeh Houshmand, Morteza Saheb Zamani, Mehdi Sedighi, "Optimization of One-Way Quantum Computation Measurement Patterns", INTERNATIONAL JOURNAL OF THEORETICAL PHYSICS, November 2018 Vol. 57, Num. 11, Page 3296-3317, November 2018,

6. Mona Arabzadeh, Morteza Saheb Zamani, Mehdi Sedighi, Sayed-Amir Marashi, "A graph-based approach to analyze flux-balanced pathways in metabolic networks", BIOSYSTEMS, January 2018 Vol. 165, Num. 0, Page 40-51, January 2018,

7. Eesa Nikahd, Mehdi Sedighi, Morteza Saheb Zamani, "Nonuniform code concatenation for universal fault-tolerant quantum computing", PHYSICAL REVIEW A, September 2017 Vol. 96, Num. 3, Page 32337-32342, September 2017,

8. Mahboobeh Houshmand Kaffashian, Mehdi Sedighi, Morteza Saheb Zamani, Koorosh Marjoei, "Quantum Circuit Synthesis Targeting to Improve One-Way Quantum Computation Pattern Cost Metrics", ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS, May 2017 Vol. 13, Num. 4, Page 0-0, May 2017,

9. Maryam Eslamy, Morteza Saheb Zamani, Mehdi Sedighi, Mahboubeh Hooshmand Kaffashian, "Optimizing Quantum Circuits Using One-Way Quantum Computation based on pattern Geometry", , February 2017 Vol. 14, Num. 4, Page 286-298, February 2017,

10. Koorosh Marjoei, Mahboobeh Houshmand Kaffashian, Morteza Saheb Zamani, Mehdi Sedighi, "Quantum-Logic Synthesis Using Improved Block-Based Approach", Iranian Journal of Electrical and Computer Engineering(IJECE), January 2017 Vol. 14, Num. 3, Page 239-248, January 2017,

11. Ghobad Zarrinchian, Morteza Saheb Zamani, "Latch-Based Structure: A High Resolution and Self-Reference Technique for Hardware Trojan Detection", IEEE TRANSACTIONS ON COMPUTERS, June 2016 Vol. PP, Num. 99, Page 1-14, June 2016,

12. Mona Arabzadeh, Mahboobeh Houshmand Kaffashian, Mehdi Sedighi, Morteza Saheb Zamani, "Quantum-Logic Synthesis of Hermitian Gates", ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS, December 2015 Vol. 12, Num. 4, Page 0-0, December 2015,

13. Mehrshad Khosraviani, Morteza Saheb Zamani, Gholamreza Bidkhori, "FogLight: an efficient matrix-based approach to construct metabolic pathways by search space reduction", BIOINFORMATICS, November 2015 Vol. 11, Num. 0, Page 1-11, November 2015,

14 Seyed Mohammad Hossein Shekarian, Morteza Saheb Zamani, "A Trust-Driven Placement Approach: A New Perspective on Design for Hardware Trust", JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS, August 2015 Vol. 24, Num. 8, Page 1-15, August 2015,

15 Eesa Nikahd, Mahboobeh Houshmand Kaffashian, Morteza Saheb Zamani, Mehdi Sedighi, "One-Way Quantum Computer Simulation", MICROPROCESSORS AND MICROSYSTEMS, March 2015 Vol. 39, Num. 3, Page 210-222, March 2015,

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17 Mahboobeh Houshmand Kaffashian, Morteza Saheb Zamani, Mehdi Sedighi, Mona Arabzadeh, "Decomposition of Diagonal Hermitian Quantum Gates Using Multiple-Controlled Pauli Z Gates", ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS, December 2014 Vol. 11, Num. 3, Page 1-10, December 2014,

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27 Hassan Ebrahimi, Morteza Saheb Zamani, Hamid Reza Zarandi, "Mitigating Soft Errors in SRAM-Based FPGAs by Decoding Configuration Bits in Switch Boxes", MICROELECTRONICS JOURNAL, January 2011 Vol. 42, Num. 1, Page 12-20, January 2011,

28 Mehdi Saeedi, Morteza Saheb Zamani, Mehdi Sedighi, Zahra Sasanian, "Reversible Circuit Synthesis Using a Cycle-Based Approach", ACM JOURNAL ON EMERGING TECHNOLOGIES IN COMPUTING SYSTEMS, December 2010 Vol. 6, Num. 4, Page 0-0, December 2010,

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34 Mehdi Saeedi, Naser Mohamadzade, Mehdi Sedighi, Morteza Saheb Zamani, "Towards A Thorough Set of Metrics for Quantum Circuit Systhesis", , February 2009 Vol. , Num. 2, Page 0-0, February 2009,

35 Ali Valizadeh, Morteza Saheb Zamani, Babak Sadeghiyan, Farhad Mehdipour, "A Reconfigurable Architecture for Implementing Multiple Cipher Algorithms", The CSI Journal on Computer Science and Engineering(JCSE), February 2009 Vol. 5, Num. 2, Page 9-15, February 2009,

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38 , Mehdi Saeedi, Morteza Saheb Zamani, "A fast IP routing lookup architecture for multi-gigabit switching routers based on reconfigurable systems", , June 2008 Vol. , Num. 32, Page 0-0, June 2008,

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43 Farhad Mehdipour, Morteza Saheb Zamani, Hamidreza Ahmadifar, T. Murakami, "An Integrated Temporal Partitioning and Physical Design Framework for Real-Time Reconfigurable Systems", , February 2006 Vol. , Num. 5, Page 0-0, February 2006,

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45 Morteza Saheb Zamani, "A specification-driven framework for the floorplanning and placement of hierarchical VLSI designs", , September 2004 Vol. , Num. 2, Page 0-0, September 2004,

Conference Papers

Portal Records

1 Milad Sharbati, Ghobad Zarrinchian, Morteza Saheb Zamani, "A Placement Method for Facilitating Detection of Hardware Trojan Horses ", Computer Society of Iran Computer Conference, March 2019

2 Sudabe Mohamadzade, Mehdi Sedighi, Morteza Saheb Zamani, "An efficient and exact synthesis of n-qubit diagonal ring gates into Clifford and T gates ", 26th Iranian Conference on Electrical Engineering, May 2018

3 Elham Ebrahimi, Saeed Shiry Ghidary, Morteza Saheb Zamani, "Fast FPGA-Based Method for Matsuoka Parameters Tuning ", International Conference on Signal Processing and Intelligent (ICSPIS), December 2016

4 Mehrnoush Moradi Haghighi, Morteza Saheb Zamani, "Soft IP Protection: An Active Approach Based on Hardware Authentication ", Iranian Conference on Electrical Engineering, May 2016

5 Maryam Eslamy, Mahboobeh Houshmand Kaffashian, Morteza Saheb Zamani, Mehdi Sedighi, "Geometry-Based Signal Shifting of One-Way Quantum Computation Measurement Patterns ", Iranian Conference on Electrical Engineering, May 2016

6 Eesa Nikahd, Mahboobeh Houshmand Kaffashian, Morteza Saheb Zamani, Mehdi Sedighi, "GOWQS: Graph-Based One-Way Quantum Computation Simulator ", Iranian Conference on Electrical Engineering, May 2016

7 Faranak Adinehzadeh, Naser Mohamadzade, Mehdi Sedighi, Morteza Saheb Zamani, "Proposing an Approach for Scheduling and Routing of Quantum Circuits with Toffoli Gates in Ion-Trap Technology ", 22nd Iranian Conference on Electrical Engineering, May 2014

8 Seyed Mohammad Hossein Shekarian, Morteza Saheb Zamani, Shirin Alsadet Aalami, "Neutralizing a Design for Hardware Trust Technique ", International Symposium on Computer Architecture and Digital Systems (CADS'13), October 2013

9 Zahra Nabizadeh.Shahrebabak, Mehdi Sedighi, Morteza Saheb Zamani, "Simultaneous Improvement of Area, Delay, and Fault Tolerance in Quantum Circuits ", International Symposium on Computer Architecture and Digital Systems (CADS'13), October 2013

10 Mina Chookhachi Zadeh Moghadam, Naser Mohamadzade, Mehdi Sedighi, Morteza Saheb Zamani, "A Hierarchical Layout Generation Method for Quantum Circuits ", International Symposium on Computer Architecture and Digital Systems (CADS'13), October 2013

11 Seyyed Ahmad Razavi Majomard, Morteza Saheb Zamani, "Improving Bitstream Compression by Modifying FPGA Architecture ", ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'13), February 2013

12 Somayeh Kashi, Morteza Saheb Zamani, "Hardware Acceleration of STON Algorithm for Comparing 3-D Structure of Proteins ", IEEE Euromicro Conference on Digital System Design (DSD'12), September 2012

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14 Mahboobeh Houshmand Kaffashian, Mohammad Hossein Samavatian, Morteza Saheb Zamani, Mehdi Sedighi, "Extracting One-way Quantum Computation Patterns from Quantum Circuits ", International Symposium on Computer Architecture and Digital Systems (CADS'12), May 2012

15 Fatemehsadat Pourhashemi Naeeni, Morteza Saheb Zamani, "Timing Yield Improvement of FPGAs Utilizing Enhanced Architectures and Multiple Configurations Under Process Variation ", ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'12), February 2012

16 Seyyed Hassan Moallem Pour, Seyyed Ahmad Razavi Majomard, Morteza Saheb Zamani, "TSV Reduction in Homogeneous 3D FPGAs by Logic Resource and Input Pad Replication ", IEEE International 3D System Integration Conference 2012 (3DIC'12), January 2012

17 Behzad Salami, Morteza Saheb Zamani, Ali Jahanian, "VMAP: A Variation Map-Aware Placement Algorithm for Leakage Power Reduction in FPGAs ", EEE Euromicro Conference on Digital System Design (DSD'11), September 2011

18 Behzad Salami, Morteza Saheb Zamani, "A Prediction Model For Estimating Leakage Power Consumption of Routing Resources in FPGAs ", Asia Symposium on Quality Electronic Design (ASQED'11), July 2011

19 Mona Arabzadeh, Morteza Saheb Zamani, Mehdi Sedighi, Mehdi Saeedi, "Logical-Depth-Oriented Reversible Logic Synthesis ", International Workshop on Logic Synthesis (IWLS'11), June 2011

20 Fatemehsadat Pourhashemi Naeeni, Morteza Saheb Zamani, "Evaluation of FPGA Routing Architectures Under Process Variation ", ACM Great Lakes Symposium on VLSI (GLSVLSI'11), May 2011

21 Hassan Ebrahimi, Morteza Saheb Zamani, Seyyed Ahmad Razavi Majomard, "A Switch Box Architecture to Mitigate Bridging Faults in SRAM-Based FPGAs ", IEEE International Symposium on Defect and Fault Tolerance (DFT10), October 2010

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30 Naser Mohamadzade, Minoo Mirsaeedi, Ali Jahanian, Morteza Saheb Zamani, "Multi-Domain Clock Skew Scheduling-Aware Register Placement to Optimize Clock Distribution Network ", Design, Automation & Test in Europe Conference, April 2009

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34 Minoo Mirsaeedi, Morteza Saheb Zamani, Mehdi Sedighi, "Multi objective statistical yield enhancement using evolutionary algorithm ", , September 2008

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43 Ali Jahanian, Morteza Saheb Zamani, Mostafa Rezvani, Mehrdad Najibi Kohneshahri, "Evaluation the metro on chip methodology to improve the congestion and routability ", , March 2008

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96 Morteza Saheb Zamani, G.R. Hellestrand, "A neural network approach to the floorplanning of hierachical VLSI designs ", , May 1995

97 Morteza Saheb Zamani, G.R. Hellestrand, "A stepwise refinement algorithm for integrated floorplanning, placement and routing of hierarchical designs ", , April 1995

Taught Courses

#	Course title	Description	Headlines	Date
1	Programmable Digital Systems Design	Modern methods for digital system design and verification		Fall 2021
2	Logic Circuits	To gain knowledge and skill to design, analyze and debug digital circuits		Fall 2021
3	Reconfigurable Systems	Introduction to reconfigurable systems and device and research topics in this field		Spring 2021
4	Programmable Digital Systems Design	Modern methods for digital system design and verification		Spring 2021
5	Logic Circuits	To gain knowledge and skill to design, analyze and debug digital circuits		Fall 2020